CLAIMS

1. A controllable current source, comprising

a first and a second supply terminal (12, 14) for the application of a first and a second supply potential (V_1, V_2), respectively,

an output terminal (16) for current delivery, which is connected via a first current path (18) with the first supply terminal (12) and via a second current path (20) with the second supply terminal (14),

with the current paths (18, 20) each having a supply side current control device (22, 24), activatable by a current control signal (S_1, S_2), as well as an output side current adjustment device (26, 28) in series to the current control device,

characterized in that the current paths (18, 20) are each allocated a potential adjustment device (40_1, 40_2), by means of which, when the current control device (22, 24) of the current path (18, 20) is inactive, a predetermined adjustment potential (V_{aa}, V_{bb}), whose value lies between the two supply potentials, is applied to an intermediate section (30, 32) lying between the current control device and the current adjustment device.

2. The controllable current source according to claim 1, wherein the current control device (22, 24) has at least one FET, whose channel forms a section of the current path (18, 20).

3. The controllable current source according to claim 1 or 2, wherein the current adjustment device (26, 28) has at least one FET, whose channel forms a section of the current path (18, 20).

4. The controllable current source according to claim 1, 2, or 3, wherein the two adjustment potentials (V_{aa}, V_{bb}) are different from one another.

5. The controllable current source according to one of the claims 1 to 4,wherein the adjustment potential (V_{aa}) for the first current path (18) lies closer to the first supply potential (V_1) than the adjustment potential (V_{bb}) for the second current path (20).

6. The controllable current source according to one of the claims 1 to 5, wherein the adjustment potential (V_{aa}, V_{bb}) for one of the two current paths (18, 20) is approximately equal to that potential which is present at the intermediate section (30, 32) of this current path (18, 20) when the current control device (22, 24) of this current path (18, 20) is activated.

7. The controllable current source according to one of the claims 1 to 6, wherein the potential adjustment device (40_1, 40_2) supplies the adjustment potential (V_{aa}, V_{bb}) between the channels of two FETs forming a voltage divider.

8. The controllable current source according to claim 7, wherein the gate terminals of the two voltage divider FETs have control signals, derived from the current control signal S_1, S_2, applied to them in such a way that, when the current control device (22, 24) is inactive, both voltage divider FETs conduct, while in contrast, when the current control device is active, both voltage divider FETs disable.

9. A controllable voltage source, comprising a controllable current source (10) according to one of the claims 1 to 8 and a downstream integrator (60).

10. A controllable oscillator device, comprising a controllable voltage source (10, 60) according to claim 9 and a downstream VCO (62).

11. A phase locked loop (50), comprising a phase detector (68), a downstream controllable oscillator device (10, 60, 62) according to claim 10, and a feedback path (64) from the oscillator device (10) to the phase detector (68).